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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,534	07/09/2003	Koay H. an Tatt	70021020-1	1966

7590 06/29/2004
AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P.O. Box 7599
Loveland, CO 80537-0599

EXAMINER

ANDUJAR, LEONARDO

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/616,534	Applicant(s) AK AN TATT ET AL.	
	Examiner Leonardo Andújar	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 May 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4 is/are rejected.
- 7) ☒ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of species 1 (claims 1 and 3) in the reply filed on 05/25/2004 is acknowledged. Nonetheless, all claims were examined on its merits because at this point the search and examination of the entire application is not a serious burden (MPEP 803).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

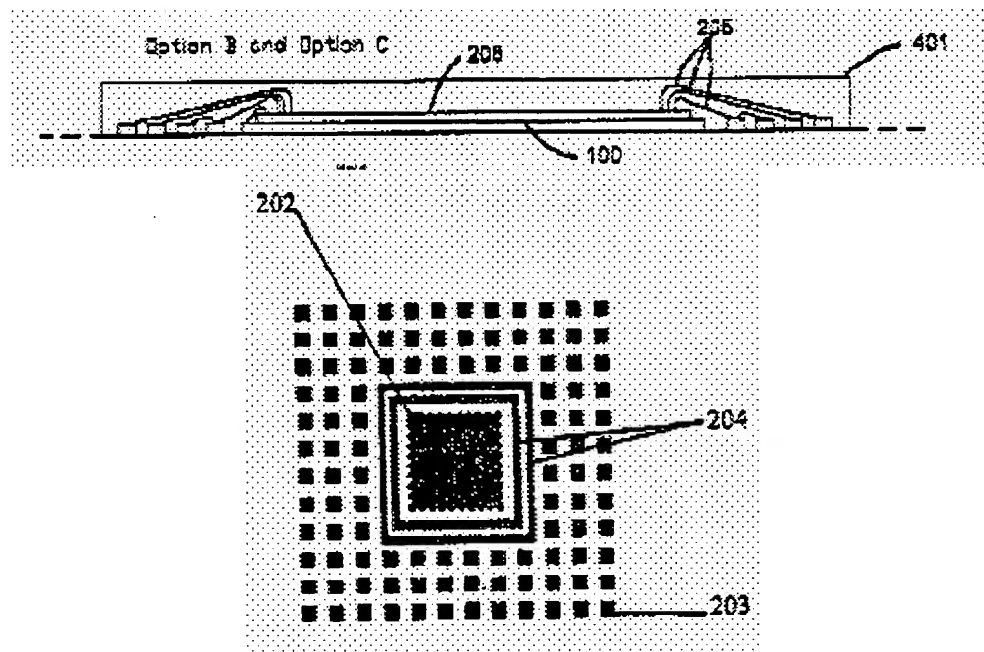
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by McLellan et al. (US 20010008305).
4. Regarding claim 1, McLellan (e.g. fig. 9) shows a package die comprising:
- A die 206 having an electrical circuit attached to a die pad 202;
 - A plurality of leads 203 arranged around the die pad, at least one of the leads being connected to the die by wires 205;
 - A power ring 204 comprising a conductor disposed between the leads and the die pad, at least one power connection 205 on the die being connected to the power ring;

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- And a layer of encapsulating material 401 covering the die, the die pad, the power ring, and the leads, the layer having a top surface, a bottom surface, and side surfaces.

McLellan, also, shows that each of the leads and the power ring comprises a conductor having a portion thereof exposed on the bottom surface.



5. Regarding claim 2, McLellan teaches that the exposed portions of the conductors may comprise solder balls 203A (e.g. fig. 6G).

6. Regarding claim 4, McLellan teaches that the leads comprises a conductor having a portion thereof that is not exposed on the bottom surface and wherein a portion of the conductor in the power ring is not exposed on the bottom surface (e.g. top portions).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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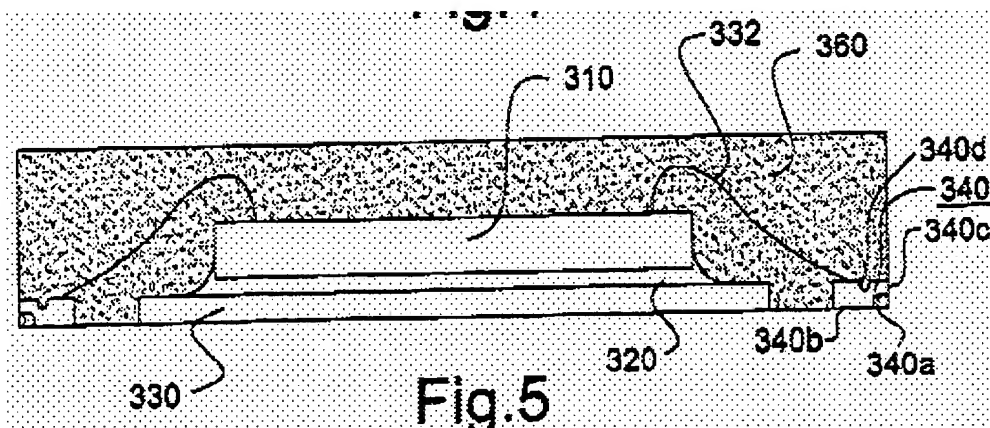
(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claim 1, 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fan et al. (US 6,400,004) in view of Templeton, Jr. et al. (US 5,457,340).

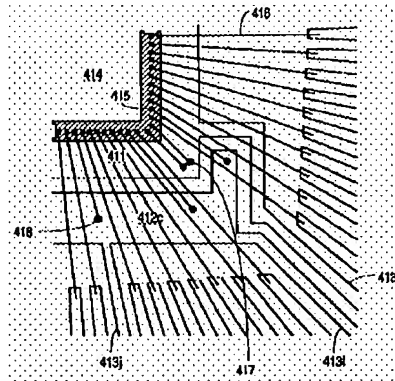
9. Regarding claim 1, Fan (e.g. figs. 1 and 2) a package die comprising:

- A die pad 330 having a die 310 having an electrical circuit thereon attached thereto;
- A plurality of I/O power leads 340 arranged around the die pad, wherein the I/O and the power leads are connected to the die by wires 332;
- And a layer of encapsulating material 360 covering the die, the die pad, and the leads, the layer having a top surface, a bottom surface, and side surfaces.

Fan, also, shows that each of the I/O and power leads comprises a conductor having a portion thereof exposed on the bottom surface.



Fan does not show that the power lead 340 comprises a power ring having a conductor disposed between the leads and the die pad. Templeton (e.g. fig. 4D) shows a package including a power ring 412 having a conductor disposed between the leads 413 and the die pad 411 wherein at least one power connection 415 of the die is connected to the power ring.



The provision of a ring in leadframes according to Templeton's disclosure allows greater flexibility in placement of ground and/or power circuit elements and bond pads on the semiconductor die. Generally, in order to minimize the length of the ground and/or power current paths (thereby minimizing inductance and, thus, noise) on an integrated circuit, it is desirable to locate ground and/or power circuit elements and bond pads on the semiconductor die in proximity to the ground and/or power lead or leads. This type of lead frame configuration results in closer placement of ground and power planes to the die than has previously been the case. Consequently, shorter bond wires are needed to make connection between bond pads on the die and the power plane. Since bond wires are a primary source of inductance because of their relative thinness, the shortening of these bond wires significantly reduces the inductance in the power and ground current paths (col. 7/lls. 2-38).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to dispose a power ring comprising a conductor between the die pad and the leads disclosed by Fan in order to reduce the inductance in the power paths because this configuration permits the use of shorter bond wires because the power plane can be located closer to the die pad as taught by Templeton.

10. Regarding claim 3, Fan shows that the die pad, and the I/O and power leads each extended to one of the side surfaces of the encapsulating material.

11. Regarding claim 4, Fan teaches that the leads comprises a conductor having a portion thereof that is not exposed on the bottom surface and wherein a portion of the conductor in the power ring is not exposed on the bottom surface (e.g. top portions).

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

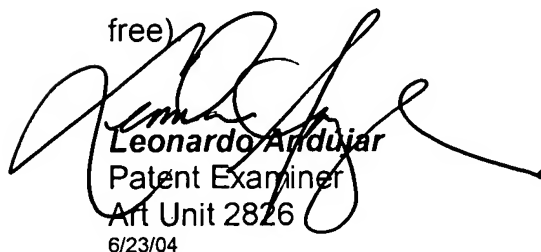
13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information

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for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-

free)



Leonardo Andujar
Patent Examiner
Art Unit 2826
6/23/04